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⑤4 Device for transforming a type "D" flip-flop into a flip-flop called type "B" able to sample data both on leading and trailing edges of the clock signal.

57) The present invention is directed to the technical field of discrete electronic components and in particular refers to a circuit device for transforming a type "D" flip-flop into a flip-flop called type "B" able to sample data both on leading and trailing edges of the clock signal, which has a first type "D" flip-flop at whose clock input is electrically connected an exclusive OR, to this first type "D" flip-flop is con-

ected a second "D"-type flip-flop identical to the first one which,being also circuitally connected with the exclusive OR output, allows to realize a flip-flop called type "B" which represents,in the wholly integrated circuitual form,a new discrete component which enables various circuitual functions not possible or not practically feasible in the prior art.

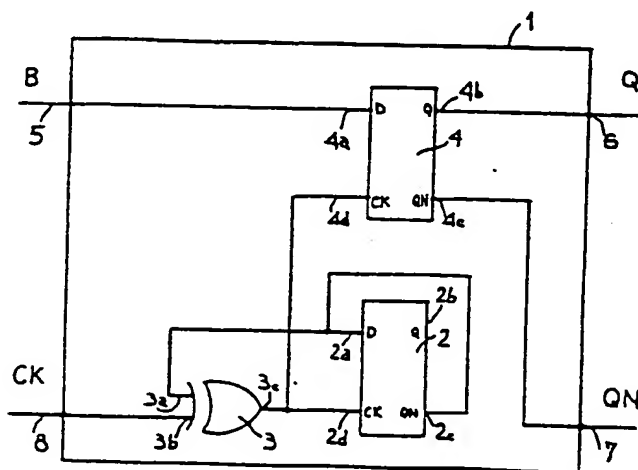


Fig. 1.

one, indicated by reference numeral 4.

The type "B" flip-flop has an input B indicated by reference numeral 5, an output Q indicated by 6, a second output QN indicated by 7, as well as a clock input indicated by 8.

The B- input 5 of type "B" flip-flop is connected directly with input D of the second type "D" flip-flop indicated by 4a, whilst the output Q of the same type "D" flip-flop, indicated by 4b, is connected directly with the Q-output 6 of type "B" flip-flop. The clock input indicated by 4d of the flip-flop 4 is connected with the output 3c of exclusive OR 3, as well as with clock input of flip-flop 2 indicated by 2d.

The output 4c of flip-flop 4 is connected directly to the output QN indicated by 7 of type "B" flip-flop.

The clock input 8 of type "B" flip-flop 1 is directly connected to one 3b of the inputs of exclusive OR 3, while the other input 3a of the same exclusive OR 3 is circuitally connected to the input D, indicated by 2a, of flip-flop 2, which input is short-circuited with the output 2c of the flip-flop itself, which represents the output QN of flip-flop 2. The output 2b, namely output Q of flip-flop 2, is not circuitally connected, while the clock input as hereinbefore mentioned, is connected with the output 3c of exclusive OR 3 and is indicated in the diagram by reference 2d.

After a description given in a mainly structural meaning, the operation of the device according to the present invention is the following.

At each clock transition we have a switching of the flip-flop 4 which acts as a divider by two and hence provides, simultaneously, for the inversion of the clock input of flip-flop 2, namely on the input 2d, thus predisposing for the subsequent transition.

Since the propagation delay normally is greater or equal to the minimum pulse width, it is clear that this last, for both flip-flops, shows the feature for which the minimum clock width depends upon propagation time of flip-flop 2 to which the delay time due to exclusive OR 3 must be added.

In more details, propagation time of flip-flop 2 coincides with the smaller time unit which can be sampled and assigned to the delay element represented by flip-flop 4, whereas the propagation time of exclusive OR 3 assures an appropriate tolerance margin.

The time setting of two flip-flops is obtained taking into consideration that the sum of propagation times of flip-flop 2 and exclusive OR 3 must be less than half the minimum duration of the pulse to be sampled.

In summary, we come to the concept that, if we neglect the exclusive OR delay time, the smaller delay time t corresponds to propagation time of flip-flop 4.

Thus the invention fully achieves the proposed objects. Indeed, in this way, it is possible to realize, in an intrinsic manner, a circuit arrangement which should require, otherwise, difficult parameters settings of the circuit itself.

Moreover, in this way there is provided a new discrete integrated component called type "B" flip-flop which, at present, is not available in the field of commercial electronic components and may be used, for instance, in the telecommunications field, as concerns the reread of data flow RZ by a clock which, through the use of a type "B" flip-flop, can work also at the same frequency of the flip-flop itself.

It is clear that the use of circuits and/or equivalent circuit components, even if structurally different, as well as technical-practical modifications, are not beyond the protective limits and the inventive sphere of the present invention, as hereinbefore described and herebelow claimed.

Claims

1. A circuit device for transforming a type "D" flip-flop into a flip-flop called type "B" able to sample data at its input both on leading and trailing edges of the clock signal, of the type comprising an exclusive OR, whose output is circuitally connected to the clock input of a first type "D" flip-flop and a delay circuit means circuitally connected to the exclusive OR too, said device being characterized in that said delay means consists of a second type "D" flip-flop whose outputs QN, Q are respectively the outputs QN, Q of the flip-flop called type "B", and whose input D is the input B of the flip-flop called type "B", and whose clock input is connected to the exclusive OR, this latter having two inputs, the first one being the clock input of the flip-flop called type "B" and the second one being circuitally connected to the input D of said first type "D" flip-flop which input D, in turn, is short-circuited with the input QN of the same flip-flop.
2. A circuit device according to claim 1, characterized in that said device is embodied as a single discrete component integrated on a chip.
3. A circuit device for transforming a type "D" flip-flop into a flip-flop called type "B" able to sample data at its input both on leading and trailing edges of the clock signal as hereinbefore described and illustrated for the proposed objects.



DOCUMENTS CONSIDERED TO BE RELEVANT			EP 90112636.7
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. CL5)
A	<u>GB - A - 2 123 634</u> (WESTERN ELECTRIC) * Fig. 1; abstract *	1	H 03 K 3/037 H 03 K 3/027 H 03 K 19/173 H 03 K 19/0175
A	<u>US - A - 4 749 937</u> (SIMONS) * Fig. 4 *	1	
A	<u>EP - A2/A3 - 0 198 677</u> (ALTERA CORP.) * Fig.4,10; abstract *	1	
A	<u>EP - A2 - 0 310 377</u> (KAWASAKI) * Fig. 4A,5A; abstract; claims *	1	
			TECHNICAL FIELDS SEARCHED (Int. CL5)
			H 03 K 3/00 H 03 K 19/00
The present search report has been drawn up for all claims			
Place of search VIENNA		Date of completion of the search 15-10-1990	Examiner BAUMANN
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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